

Appl. No : 09/262,000
Amdt. dated : 09/08/03
Reply to Office Action of 05/08/03

Amendments to the Claims:

This listing will replace all prior versions, and listing, of claims in the application.

K2
8. (currently amended) A method of forming a device structure that combines insulating materials for alignments posts and optical interference layers associated with an active device structure in a silicon body comprising:

providing a silicon wafer having a pattern of active device structures therein and thereon;

forming a first metallic layer over the surface of said wafer;

forming a second metallic layer over said first metallic layer, which is used both for connections and for bonding pads;

forming a silicon dioxide insulation over said second metallic layer;

forming a third metallic layer over said layer of silicon dioxide;

forming a photoresist mask over said third metallic layer having a covering over planned pixel locations of said liquid-crystal-on-silicon display device;

Appl. No : 09/262,000

Amdt. dated : 09/08/03

Reply to Office Action of 05/08/03

removing said third metallic layer not covered by said
photoresist mask[, forming said alignment posts whereby said
alignment post are formed by the process of amorphous silicon by
plasma etching upon said silicon substrate];

removing said photoresist mask to provide that each said
pixel retains said third metallic layer, which shall act as a
mirror reflector for light incident upon said liquid-crystal-on-
silicon display device; [[and]]

depositing optical interference layers of silicon oxide or
silicon nitride [or silicon oxide or silicon nitride] over said
third metallic layer and said silicon dioxide layer; and

forming said alignment posts whereby said alignment post
are formed by the process of amorphous silicon by plasma etching
upon said silicon substrate.

Claims 9-13: (cancelled).

14. (currently amended) The method of claim 8 [[for]] further
comprising forming an amorphous silicon layer of thickness
between about 0.1 and 5 microns to achieve the desired height of
the alignment posts.

15. (currently amended) The method of claim 8 [[for]] further
comprising forming a photoresist mask over said amorphous

Appl. No : 09/262,000
Amdt. dated : 09/08/03
Reply to Office Action of 05/08/03
silicon layer to cover the location of each planned alignment post.

16. (currently amended) The method of claim 8 [[for]] further comprising removing said amorphous silicon to form said alignment posts by plasma etch, and removing said photoresist mask.

Claim 17: (cancelled)

18. (currently amended) The method of claim 38 [[for]] further comprising forming a PECVD oxide layer of thickness between 0. 1 and 5 microns to achieve the desired height of the alignment posts.

19. (currently amended) The method of claim [38 for] 18 further comprising forming a photoresist mask over said PECVD oxide layer to expose the location of each planned alignment post.

20. (currently amended) The method of claim [38 for] 19 further comprising forming post cavities by plasma etching of said PECVD oxide layer.

Appl. No : 09/262,000
Amdt. dated : 09/08/03
Reply to Office Action of 05/08/03

(R)

21. (currently amended) The method of claim [38 for] 20 further comprising plasma enhanced chemical vapor deposition of silicon nitride into said post cavities.

22. (currently amended) The method of claim [38 for] 21 further comprising etch-back removal of said silicon nitride, except that silicon nitride deposited in said post cavities.

23. (currently amended) The method of claim [38 for] 22 further comprising removing the PECVD oxide layer by wet etch (such as HF or buffered HF) to form said silicon nitride alignment posts, and removing said photoresist mask.

Claim 24: (cancelled).

25. (currently amended) The method of claim 39 wherein a two-micron bottom photoresist layer or PMMA acylic layer [of thickness between about 1 and 5 microns] is deposited upon the OIL and covered by silicon monoxide via thermal evaporation, followed by another photoresist layer [of thickness between about 0.1 and 1 micron].

Appl. No : 09/262,000
Amdt. dated : 09/08/03
Reply to Office Action of 05/08/03

26. (currently amended) The method of claim [[39]] 25 wherein a photomask is used to form [[said]] cavities in said silicon monoxide by a CF₄ plasma etching of the silicon monoxide, after which the silicon monoxide serves as a mask for an oxygen plasma etching of said two-micron bottom photoresist or PMMA acylic layer.

27. (currently amended) The method of claim [39 for] 26 further comprising forming an insulation material by plug filling the cavities formed in the silicon monoxide and two-micron bottom photoresist layer or PMMA acylic layer; several insulation materials are available from which to choose, including calcium fluoride, silicon monoxide, yttrium oxide, and aluminum oxide, and the like.

28. (currently amended) The method of claim [39 for] 27 further comprising removing said bottom photoresist layer or PMMA acylic layer by lift-off with an ultrasonic bath, leaving said alignment posts.

Claim 29: (cancelled).

Appl. No : 09/262,000
Amdt. dated : 09/08/03
Reply to Office Action of 05/08/03

30. (currently amended) The method of claim 40 [[for]] further comprising forming a photosensitive polyimide layer of thickness between about 0.1 and 5 microns [posts] to achieve the desired height of the alignment posts.

31. (currently amended) The method of claim [40 for] 30 further comprising exposing said photosensitive polyimide at the location of each planned alignment post.

32. (currently amended) The method of claim [40 for] 31 further comprising developing and removing said photosensitive polyimide to leave said alignment posts in the location of the exposed polyimide described herein, and removing said photoresist mask.

Claims 33-37: (cancelled)

38. (currently amended) A method of forming a device structure that combines insulating materials for alignments posts and optical interference layers associated with an active device structure in a silicon body comprising:

providing a silicon wafer having a pattern of active device structures therein and thereon;

Appl. No : 09/262,000
Amdt. dated : 09/08/03
Reply to Office Action of 05/08/03

forming a first metallic layer over the surface of said wafer;

forming a second metallic layer over said first metallic layer, which is used both for connections and for bonding pads;

forming a silicon dioxide insulation over said second metallic layer;

forming a third metallic layer over said layer of silicon dioxide;

forming a photoresist mask over said third metallic layer having a covering over planned pixel locations of said liquid-crystal-on-silicon display device;

removing said third metallic layer not covered by said photoresist mask[, forming said alignment posts by the process of silicon nitride by plug filling upon the silicon substrate];

removing said photoresist mask to provide that each said pixel retains said third metallic layer, which shall act as a mirror reflector for light incident upon said liquid-crystal-on-silicon display device; [[and]]

depositing optical interference layers of silicon oxide or silicon nitride [or silicon oxide or silicon nitride] over said third metallic layer and said silicon dioxide layer; and

forming said alignment posts by the process of silicon nitride by plug filling upon the silicon substrate.

X/R
39. (currently amended) A method of forming a device structure that combines insulating materials for alignments posts and optical interference layers associated with an active device structure in a silicon body comprising:

providing a silicon wafer having a pattern of active device structures therein and thereon;

forming a first metallic layer over the surface of said wafer;

forming a second metallic layer over said first metallic layer, which is used both for connections and for bonding pads;

forming a silicon dioxide insulation over said second metallic layer;

forming a third metallic layer over said layer of silicon dioxide;

forming a photoresist mask over said third metallic layer having a covering over planned pixel locations of said liquid-crystal-on-silicon display device;

removing said third metallic layer not covered by said photoresist mask[, forming said alignment post by the process of

Appl. No : 09/262,000
Amdt. dated : 09/08/03
Reply to Office Action of 05/08/03

insulation material by lift-off upon said optical interference layer OIL];

PT

removing said photoresist mask to provide that each said pixel retains said third metallic layer, which shall act as a mirror reflector for light incident upon said liquid-crystal-on-silicon display device; [[and]]

depositing optical interference layers of silicon oxide or silicon nitride [or silicon oxide or silicon nitride] over said third metallic layer and said silicon dioxide layer; and

forming said alignment post by the process of insulation material by lift-off upon said optical interference layer.

40. (currently amended) A method of forming a device structure that combines insulating materials for alignments posts and optical interference layers associated with an active device structure in a silicon body comprising:

providing a silicon wafer having a pattern of active device structures therein and thereon;

forming a first metallic layer over the surface of said wafer;

forming a second metallic layer over said first metallic layer, which is used both for connections and for bonding pads;

Appl. No : 09/262,000
Amdt. dated : 09/08/03
Reply to Office Action of 05/08/03

forming a silicon dioxide insulation over said second metallic layer;

forming a third metallic layer over said layer of silicon dioxide;

forming a photoresist mask over said third metallic layer having a covering over planned pixel locations of said liquid-crystal-on-silicon display device;

removing said third metallic layer not covered by said photoresist mask[, forming said alignment post by a process of polyimide by photosensitive etching upon an Optical Interference Layer (OIL)];

removing said photoresist mask to provide that each said pixel retains said third metallic layer, which shall act as a mirror reflector for light incident upon said liquid-crystal-on-silicon display device; [[and]]

depositing optical interference layers of silicon oxide or silicon nitride [or silicon oxide or silicon nitride] over said third metallic layer and said silicon dioxide layer; and

forming said alignment post by a process of polyimide by photosensitive etching upon an Optical Interference Layer (OIL).